

RELIABILITY OF SUPER LOW NOISE HEMTS

Kazuo Hayashi, Takuji Sonoda, Tetsuya Yamaguchi, +Kohki Nagahama,
Masahide Yamanouchi, Saburou Takamiya, and Sigeru Mitsui

Kita-Itami Works,
+ LSI Research and Development Laboratory,
Mitsubishi Electric Corporation
4-1 Mizuhara, Itami, 664 Japan

ABSTRACT

The first report on a comprehensive study of the reliability of super low noise HEMTs with a typical noise figure of 1.2 dB at 12GHz is presented. No failure was observed in both DC running and high temperature storage tests during 2000 hours. These successful results were achieved by a newly developed low temperature ohmic sintering technology and a novel Ni/Al gate.

INTRODUCTION

High electron mobility transistors (HEMTs) have demonstrated their capabilities as high speed and low noise devices. Recently, in the field of microwave low noise amplification, HEMTs have become increasingly popular as possible replacements for the conventional GaAs MESFETs [1]-[3]. However, some problems related to the reliability of HEMTs have been remained, which have to be solved before using HEMTs in commercial communication systems. In fact, there are no reports about high reliability HEMTs available. We present the first report on a comprehensive study of the reliability of HEMTs.

There are mainly two problems related to the HEMTs' reliability. One problem is the lateral migration of ohmic contact constituents into the channel region and non uniform surface morphology by the conventional high temperature ohmic sintering for HEMTs[4]. The other is a non-pinch-off failure reported about the submicron pure Al gate widely used for HEMTs[5].

We have developed a low temperature sintering process and a novel gate with Ni under the Al in order to solve the problems related to the reliability of HEMTs. A DC operational life test under four bias conditions of $V_{ds}=2.5, 3.0, 4.0, 5.0$ V, $I_{ds}=30$ mA respectively and a high temperature storage test at 200°C in a nitrogen atmosphere were carried out.

DEVICE FABRICATION

HEMT structures were grown by a specially designed automatic MBE system. This system can grow very pure and extremely uniform epitaxial layers on up to seven 2-in. wafers at a time. As shown in Fig.1, the epitaxial structure consists of an undoped GaAs buffer layer, a Si-doped $Al_{0.3}Ga_{0.7}As$ layer, and a Si-doped GaAs cap layer in order to obtain a low source-drain contact resistance. A typical doping concentration in AlGaAs layer is $2 \times 10^{18} \text{ cm}^{-3}$. The devices have a source-to-drain spacing of $3 \mu\text{m}$ and a total gate width of $200 \mu\text{m}$. $0.4 \mu\text{m}$ gates are formed by using Deep UV photolithography followed by a lift off technique, and then are sintered at 280 °C. The gate region is recessed to the optimum depth by wet chemical etching, which can achieve both a high gate breakdown voltage and a super low noise performance. Devices are passivated by a layer of PECVD silicon nitride. The HEMT chips are assembled into hermetically sealed packages in order to evaluate DC and RF characteristics.

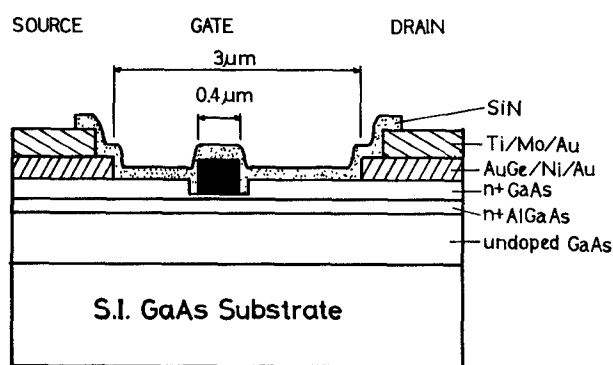


Fig.1 Schematic cross-sectional view of HEMT.

EXPERIMENTAL RESULTS

Packaged HEMTs reproducibly exhibited a typical noise figure (NF) of 1.2 dB with an associated gain of 10.5 dB at 12GHz. Fig.2 show NF histograms of the HEMTs under the bias condition of $V_{ds}=2.0V$, $I_{ds}=7.5mA$. Lot No.A and No.B samples in Fig.2 were fabricated by same epitaxial grown batch and different process batches. The average NF (\overline{NF}) and the standard deviation (σ) for the two samples are much the same. These results indicate that our newly developed process technology for HEMTs is highly reproducible and HEMT structures grown by the specially designed high throughput MBE system are extremely uniform. Furthermore, as shown in Fig.3 and Fig.4, these HEMTs showed good pinch off characteristics even in the bias condition of $V_{ds}=5.0V$, which are due to high gate breakdown voltage over 10V.

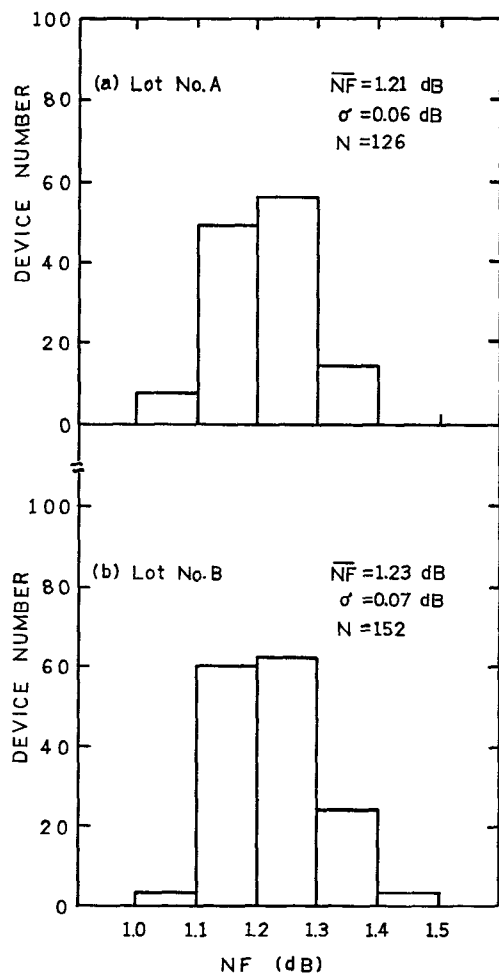


Fig.2 Histograms of noise figures (NF) for HEMTs of Lot No.A and No.B.

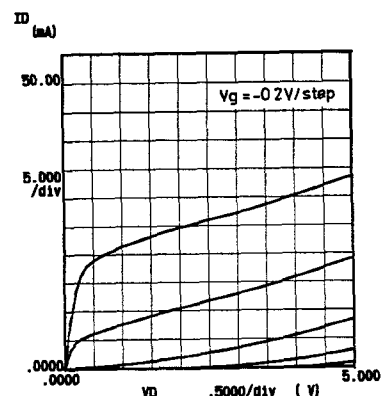


Fig.3 Drain I-V characteristics.

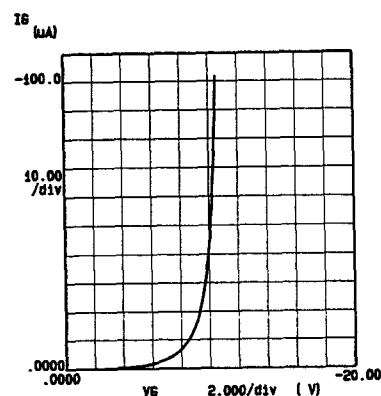


Fig.4 Gate-drain reverse I-V characteristics

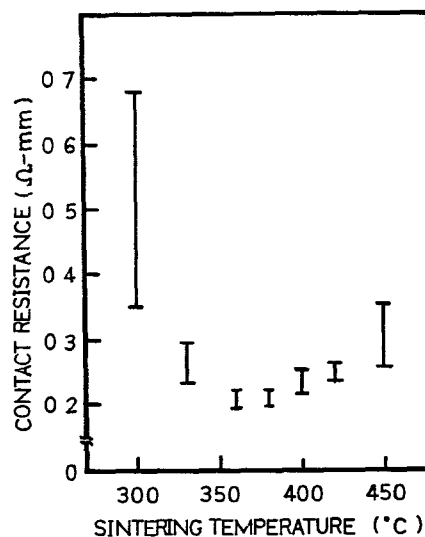


Fig.5 Variation of contact resistance with sintering temperature for HEMT.

Fig.5 shows that extremely low contact resistances for source and drain electrodes were achieved by a low temperature sintering (360-380 °C). The low temperature sintering also allowed uniform surface morphology. These results were obtained by the optimization of the ohmic metal composition (AuGe/Ni/Au) and the sintering profile (sintering temperature and sintering time).

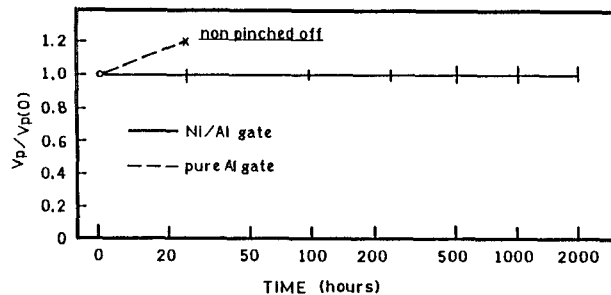


Fig.6 Aging characteristics of pinch off voltage (V_p) during DC operational life test ($V_{ds}=5.0V$, $I_{ds}=30mA$).

A DC operational life test under the bias condition of $V_{ds}=5V$, $I_{ds}=30mA$ was carried out. In the case of the Ni/Al gate HEMTs, no failure modes were observed during the 2000 hours DC operational life test. As an example, Fig.6 shows stable aging characteristics of pinch-off voltage in the Ni/Al gate HEMTs. On the other hand, in the pure Al gate HEMTs, the non-pinch-off failure was observed (Fig.6). Fig.7 and Fig.8 indicate the Auger depth profiles before and after gate-sintering respectively. These results suggest that the formation of a stable NiAl alloy effectively suppress the electromigration. As a result, not only non-pinch-off failure but also any other failure modes were not observed in the HEMT using the Ni/Al alloyed gate.

In the HEMT with the novel gate, saturated drain current (I_{dss}) increased by the gate-sintering process at 280 °C. This phenomenon can be explained by the decrease of the schottky barrier height due to alloying Ni and Al. However, after the gate-sintering, DC and RF characteristics were stable and were not affected by the 2000 hours high temperature storage test even at 200 °C. Fig.9 and Fig.10 demonstrate stable I_{dss} and NF of the HEMT with the Ni/Al alloyed gate during the 2000 hours high temperature storage test at 200°C.

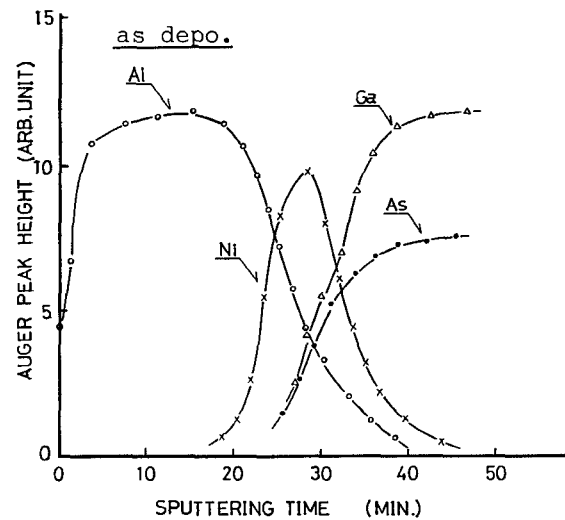


Fig.7 Auger depth profile before sintering.

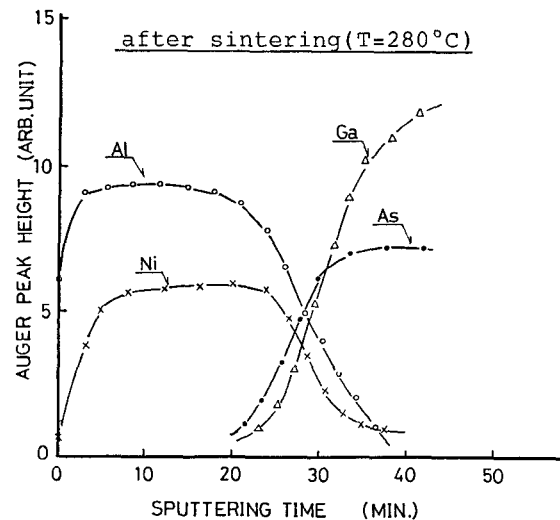


Fig.8 Auger depth profile after sintering.

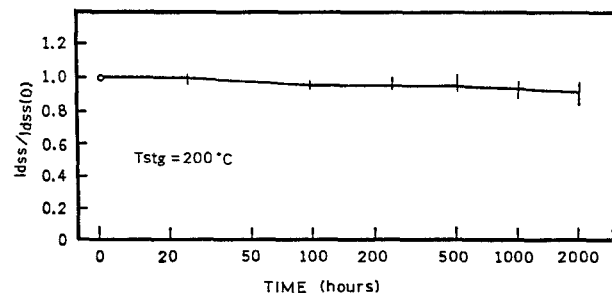


Fig.9 Aging characteristics of saturated drain current (I_{dss}) during high temperature storage test.

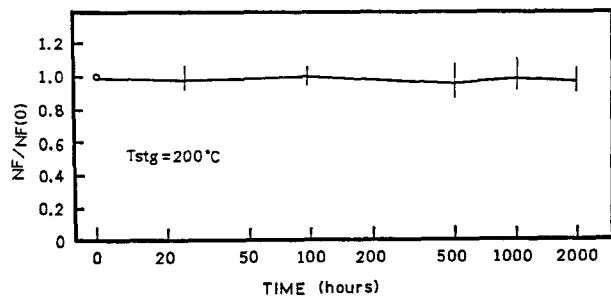


Fig.10 Aging characteristics of noise figure (NF) during high temperature storage test.

- [5] K.Katsukawa, et al., "Reliability of Gate Metallization in Power GaAs MESFETs," 22nd Annu. Proc. Reliability Physics, pp.59-62, 1984.

CONCLUSION

For the first time, super low noise HEMTs with high reliability and excellent reproducibility were fabricated. These results were achieved by using the low temperature ohmic sintering technology and the Ni/Al alloyed gate combined the newly developed high throughput MBE system. These HEMTs have been stably operating at present to 2000 hours in the hard stress condition.

ACKNOWLEDGEMENT

The authors would like to thank Dr. T.Murotani and R.Hirano for supporting and encouraging their work. They also wish to thank M.Odaka and H.Kurokawa for Auger analysis. Thanks are also due to K.Kusunoki, A.Nara, T.Suzuki and all the staff concerned at the High Frequency Devices Division, Mitsubishi Electric Corp., for their kind advice and cooperation.

REFERENCES

- [1] K.Joshin, et al., "Noise Performance of Microwave HEMT," Proc. 1983 IEEE MTT-S Int'l. Microwave Symp., pp.563-565, 1983.
- [2] T.Mochizuki, et al., "Low Noise Amplifiers Using Two Demensional Electron Gas FETs," Proc. 1985 IEEE MTT-S Int'l. Microwave Symp., pp.543-546, 1985.
- [3] K.Shibata, et al., "20 GHz-Band Low Noise HEMT Amplifier," Proc.1986 IEEE MTT-S Int'l. Microwave Symp., pp.75-78, 1986.
- [4] A.Christou, et al., "Failure Mechanism Study of GaAs MODFET Devices and Integrated Circuits," IEEE 23rd Annu. Proc. Reliability Physics, pp.54-59, 1985.